Loop Optimizations

Instruction Scheduling
Outline

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• Hardware vs. Compiler
• Induction Variable Recognition
• loop invariant code motion
Scheduling Loops

• Loop bodies are small
• But, lot of time is spent in loops due to large number of iterations
• Need better ways to schedule loops
Loop Example

• Machine
  – One load/store unit
    • load 2 cycles
    • store 2 cycles
  – Two arithmetic units
    • add 2 cycles
    • branch 2 cycles
    • multiply 3 cycles
  – Both units are pipelined (initiate one op each cycle)

• Source Code
  
  ```
  for i = 1 to N
  ```
Loop Example

• Source Code

```c
for i = 1 to N
```

• Assembly Code

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```

(base, offset)
Loop Example

• Assembly Code

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```

```assembly
imul
2

mov
3

imul
0

mov
2

sub
2

jz
2

mov
d=7

imul
d=5

mov
d=2

sub
d=2

jz
d=0

mov
d=0
```
Loop Example

• Assembly Code
  loop:
  mov (%rdi, %rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi, %rax)
  sub $4, %rax
  jz loop

• Schedule (9 cycles per iteration)
Outline

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Loop Unrolling

• Unroll the loop body few times
• Pros:
  – Create a much larger basic block for the body
  – Eliminate few loop bounds checks
• Cons:
  – Much larger program
  – Setup code (# of iterations < unroll factor)
  – beginning and end of the schedule can still have unused slots
Loop Example

loop:
  mov   (%rdi,%rax), %r10
  imul  %r11, %r10
  mov   %r10, (%rdi,%rax)
  sub   $4, %rax
  jz    loop
Loop Example

```
loop:
    mov  (%rdi,%rax), %r10
    imul %r11, %r10
    mov  %r10, (%rdi,%rax)
    sub  $4, %rax
    mov  (%rdi,%rax), %r10
    imul %r11, %r10
    mov  %r10, (%rdi,%rax)
    sub  $4, %rax
    jz    loop
```
Loop Example

```
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
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    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```

- Schedule (8 cycles per iteration)

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Loop Unrolling

• Rename registers
  – Use different registers in different iterations
Loop Example

```assembly
loop:
  mov (%rdi,%rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi,%rax)
  sub $4, %rax
  mov (%rdi,%rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi,%rax)
  sub $4, %rax
  jz loop
```

Loop Example

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    mov (%rdi,%rax), %rcx
    imul %r11, %rcx
    mov %rcx, (%rdi,%rax)
    sub $4, %rax
    jz loop
```
Loop Unrolling

• Rename registers
  – Use different registers in different iterations

• Eliminate unnecessary dependencies
  – again, use more registers to eliminate true, anti and output dependencies
  – eliminate dependent-chains of calculations when possible
Loop Example

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    mov (%rdi,%rax), %rcx
    imul %r11, %rcx
    mov %rcx, (%rdi,%rax)
    sub $4, %rax
    jz loop
```
Loop Example

loop:
  mov  ( %rdi , %rax ) , %r10
  imul %r11 , %r10
  mov %r10 , ( %rdi , %rax )
  sub $8 , %rax
  mov  ( %rdi , %rbx ) , %rcx
  imul %r11 , %rcx
  mov %rcx , ( %rdi , %rbx )
  sub $8 , %rbx
  jz  loop
Loop Example

```plaintext
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $8, %rax
    mov (%rdi,%rbx), %rcx
    imul %r11, %rcx
    mov %rcx, (%rdi,%rbx)
    sub $8, %rbx
    jz loop
```

- Schedule (4.5 cycles per iteration)

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Outline

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• Hardware vs. Compiler
• loop invariant code motion
• Induction Variable Recognition
Software Pipelining

• Try to overlap multiple iterations so that the slots will be filled

• Find the steady-state window so that:
  – all the instructions of the loop body is executed
  – but from different iterations
Loop Example

• **Assembly Code**

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```

• **Schedule**

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Loop Example

• Assembly Code
  
  loop:
  mov   (%rdi,%rax), %r10
  imul  %r11, %r10
  mov   %r10, (%rdi,%rax)
  sub   $4, %rax
  jz    loop

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Loop Example

• Assembly Code

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loop:
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```

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Loop Example

• Assembly Code

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# Loop Example

## Assembly Code

```assembly
loop:
    mov (%rdi,%rax), %r10
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    jz loop
```

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```
Loop Example

- **Assembly Code**

  ```assembly
  loop:
  mov (%rdi,%rax), %r10
  imul %r11, %r10
  mov %r10, (%rdi,%rax)
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  jz loop
  ```

- **Schedule**

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## Loop Example

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Schedule Example
Loop Example

• Assembly Code

   loop:
   mov (%rdi,%rax), %r10
   imul %r11, %r10
   mov %r10, (%rdi,%rax)
   sub $4, %rax
   jz loop

• Schedule (2 cycles per iteration)
Loop Example

• 4 iterations are overlapped
  – value of $r11$ don’t change
  – 4 regs for ($rdi, rax$)
  – each addr. incremented by $4*4$
  – 4 regs to keep value $r10$

– Same registers can be reused after 4 of these blocks
  generate code for 4 blocks, otherwise need to move

```assembly
loop:
    mov (%rdi,%rax), %r10
    imul %r11, %r10
    mov %r10, (%rdi,%rax)
    sub $4, %rax
    jz loop
```
Software Pipelining

• Optimal use of resources
• Need a lot of registers
  – Values in multiple iterations need to be kept
• Issues in dependencies
  – Executing a store instruction in an iteration before branch instruction is executed for a previous iteration (writing when it should not have)
  – Loads and stores are issued out-of-order (need to figure-out dependencies before doing this)
• Code generation issues
  – Generate pre-amble and post-amble code
  – Multiple blocks so no register copy is needed
Outline

- Scheduling for loops
- Loop unrolling
- Software pipelining
- **Interaction with register allocation**
- Hardware vs. Compiler
- Induction Variable Recognition
- loop invariant code motion
Register Allocation and Instruction Scheduling

• If register allocation is before instruction scheduling
  – restricts the choices for scheduling
Example

1: mov 4(%%rbp), %rax
2: add %rax, %rbx
3: mov 8(%%rbp), %rax
4: add %rax, %rcx
Example

1: mov 4(\%rbp), \%rax
2: add \%rax, \%rbx
3: mov 8(\%rbp), \%rax
4: add \%rax, \%rcx
Example

1: mov 4(%rbp), %rax
2: add %rax, %rbx
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Example

1: mov 4(%rbp), %rax
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Anti-dependence
How about a different register?
Example

1: mov 4(%rbp), %rax
2: add %rax, %rbx
3: mov 8(%rbp), %r10
4: add %r10, %rcx

Anti-dependence
How about a different register?
### Example

1: `mov 4(%rbp), %rax`
2: `add %rax, %rbx`
3: `mov 8(%rbp), %r10`
4: `add %r10, %rcx`

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>MEM 1</td>
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<td>3</td>
</tr>
<tr>
<td>MEM 2</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>
Register Allocation and Instruction Scheduling

• If register allocation is before instruction scheduling
  – restricts the choices for scheduling
Register Allocation and Instruction Scheduling

- If register allocation is before instruction scheduling
  - restricts the choices for scheduling

- If instruction scheduling is before register allocation
  - Register allocation may spill registers
  - Will change the carefully done schedule!!!
Outline

• Scheduling for loops
• Loop unrolling
• Software pipelining
• Interaction with register allocation
• Hardware vs. Compiler
• Induction Variable Recognition
• loop invariant code motion
Superscalar: Where have all the transistors gone?

• Out of order execution
  – If an instruction stalls, go beyond that and start executing non-dependent instructions
  – Pros:
    • Hardware scheduling
    • Tolerates unpredictable latencies
  – Cons:
    • Instruction window is small
Superscalar: Where have all the transistors gone?

• Register renaming
  – If there is an anti or output dependency of a register that stalls the pipeline, use a different hardware register
  – Pros:
    • Avoids anti and output dependencies
  – Cons:
    • Cannot do more complex transformations to eliminate dependencies
Hardware vs. Compiler

- In a superscalar, hardware and compiler scheduling can work hand-in-hand
- Hardware can reduce the burden when not predictable by the compiler
- Compiler can still greatly enhance the performance
  - Large instruction window for scheduling
  - Many program transformations that increase parallelism
- Compiler is even more critical when no hardware support
  - VLIW machines (Itanium, DSPs)